IG-NANA

The best of GOI / COP free / Gettering
Process Flow of IG-NANA Wafer

1. Crystal Growth
   - Nitrogen doped Si Crystal
   - Si Melt
2. Wafering
3. High Temp. Annealing (Surface Improvement)
4. IG-NANA Wafer

Steps:
- Slicing
- Polishing
- Argon Annealing
- Polished Wafer
IG-NANA Wafer
High performance and Cost-effective Wafer.
The best starting material for variety of device process including Low Thermal Budget.

Summary

Surface:Defect Free

Bulk:Gettering Effect

Silicon Wafer

Cross-sectional View

<table>
<thead>
<tr>
<th></th>
<th>IG-NANA</th>
<th>Thin Epi</th>
<th>CZ/RTA</th>
<th>HAW</th>
<th>Pure</th>
<th>CZPW</th>
</tr>
</thead>
<tbody>
<tr>
<td>Surface Defect &amp; COP</td>
<td>Excellent</td>
<td>Excellent</td>
<td>Good</td>
<td>Good</td>
<td>Excellent</td>
<td>Fair</td>
</tr>
<tr>
<td>Gettering Performance</td>
<td>Excellent</td>
<td>Good</td>
<td>Good</td>
<td>Fair</td>
<td>Fair</td>
<td>Fair</td>
</tr>
</tbody>
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150～200mm wafer : Mass production
300mm wafer : Under development and sample-scale production

Perfect Denuded Zone

CZ PW
133 defects/cm²

IG-NANA
0.30 defects/cm²

Measured by LSTD scanner, detecting 0~5μm near surface larger than 50nm
High Performance for Junction Leakage

Correlation between the number of high leakage cell and LSTD density
(Source: H. Kubota et al., E.C.S. Proceedings Vol. 2000 -17)

Deeper COP free zone

Deeper high TDDB zone

after Low Thermal Budget process measured by Shin Etsu STD method

IG-NANA Low Cl | IG-NANA High Cl | CZ/RTA
IG-NANA Mid Cl | Low Defect CZ | HAW
**What is NANA?**

NANA means "7" in Japanese. This is the atomic number of Nitrogen. The NANA is symbolic of nitrogen doping technology.

- NANA technology is the solution for achieving
  1. The higher gettering performance by BMD
  2. The perfect Denuded Zone for device region

- Shin-Etsu Handotai (SEH) provides two types of NANA wafers, **IG-NANA / EP-NANA**

  to satisfy all requirements in sub-0.25μm device generation and beyond.

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**Development History**

**Gettering Problems**

1977 Invention of Intrinsic Gettering (IG)
1983 ~ Development of DZ-IG wafer
1993 ~ Gettering trouble due to lowered Oxygen
1994 ~ Increasing need for P/P- Epi wafer to avoid COP
1995 ~ Problem due to poor gettering ability of P/P- Epi

**2000 ~ SEH IG-NANA for ultimate solution**

1997 Evidence of residual COPs on hydrogen annealed wafer
1991 ~ Development of hydrogen annealed wafer to avoid COP
1991 Device failure due to COPs with shrinking design rule
1990 Discovery of COPs as a grown-in defect
1983 ~ GOI problem due to Grown-in Defects

**COPs Problems**
Precaution

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