SOI Wafer
Solution for High Speed / Low Power Consumption
UNIBOND® Wafers

Smart-Cut® SOI Process for UNIBOND® Wafers

Specifications

- **Standard**
  - Diameter: 200 mm
  - SOI:
    - thickness: 100~200 nm
    - uniformity: < ±5%
    - type: P-type
    - resistivity: 8.5~11.5 Ω cm
    - orientation: Notch/Flat: Notch
  - BOX:
    - thickness: 400 nm
    - uniformity: < ±2.5%
  - Base wafer:
    - thickness: 725 μm
    - type: P-type
    - resistivity: 14~22 Ω cm
    - orientation: < 100 >
  - HF defect: < 0.3/cm²
  - Secco defect: 1×10⁻⁸/cm²
  - Pipe density: none
  - Roughness(rms): < 0.2 nm
  - Metal contamination: < 2×10⁻¹⁰/cm²
  - Edge exclusion: 5 mm

- **Customized**
  - Diameter: 200 mm
  - SOI:
    - thickness: 80~1000 nm
    - uniformity: < ±5%
    - type: P-type
    - resistivity: Arbitrary
    - orientation: < 100 >
  - BOX:
    - thickness: 100~3000 nm
    - uniformity: < ±2.5%
  - Base wafer:
    - thickness: 725 μm
    - type: P-type
    - resistivity: Arbitrary
    - orientation: < 100 >
  - HF defect, Secco defect: to be specified
  - Pipe density: none
  - Roughness(rms): < 0.2 nm
  - Metal contamination: < 2×10⁻¹⁰/cm²
  - Edge exclusion: 5 mm

**Note:** 300mm UNIBOND® wafers are under development.
SOI Wafers are promising material

SOI wafer is total solution material to realize high speed, low power consumption and leak tight due to ideal isolation. It provides flexibility and enhancement for IC designs and development.

SEH Supplies SOI Wafers on Your Requirements

Features of SEH SOI Wafers

1. Excellent thickness uniformity of SOI layer
2. SOI crystal quality equivalent to bulk Si wafer
3. BOX quality equivalent to thermal oxide
4. Low cost and volume supply

Typical Applications

1. High speed / low power / low voltage ICs
2. System-On-Chip
3. High-temperature electronics
4. Radiation-hardened circuits
5. Smart power devices
6. Smart sensors

Options

SEH supplies SOI wafers as customers' requirements.

1. SOI layer thickness and resistivity
2. Specification of base and bond wafer
3. Buried oxide layer thickness
### Bonded & Polished SOI (BPSOI) Wafers

#### Process for BPSOI

- **Oxidation**
  - Bond wafer
  - Base wafer

- **Cleaning & Bonding at RT Annealing (1100°C, 2hr, O₂)**

- **Grinding**
  - t = 10 – 20 μm

- **Polishing**
  - t ≥ 1 μm

- **SOI**

- **Bonded SOI**

- **Buried oxide**

#### Specifications

##### Standard BPSOI Layer

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Diameter</td>
<td>100, 125, 150, 200 mm</td>
</tr>
<tr>
<td>Crystal orientation</td>
<td>&lt; 100 &gt; &lt; 110 &gt; &lt; 111 &gt;</td>
</tr>
<tr>
<td>Dopant</td>
<td>N Type (P, Sb), P Type (B)</td>
</tr>
<tr>
<td>SOI layer thickness</td>
<td>1.0 μm or thicker</td>
</tr>
<tr>
<td>SOI thickness uniformity</td>
<td>+/-0.5 μm</td>
</tr>
<tr>
<td></td>
<td>(premium for +/-0.3 μm)</td>
</tr>
<tr>
<td>Buried oxide</td>
<td>0.1 μm ~ 4 μm</td>
</tr>
<tr>
<td>Buried oxide thickness uniformity</td>
<td>+/-5%</td>
</tr>
<tr>
<td>Crystal quality</td>
<td>Bulk level</td>
</tr>
<tr>
<td>Surface quality</td>
<td>Polished wafer level</td>
</tr>
</tbody>
</table>

##### Standard Base Wafer

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Orientation</td>
<td>&lt; 100 &gt;</td>
</tr>
<tr>
<td>Dopant</td>
<td>N Type (P, Sb), P Type (B)</td>
</tr>
<tr>
<td>Resistivity</td>
<td>P (1 ~ 30 Ωcm) +/-40%,</td>
</tr>
<tr>
<td></td>
<td>Sb (0.01 ~ 0.05 Ωcm) +/-30%</td>
</tr>
<tr>
<td></td>
<td>B (0.01 ~ 0.05 Ωcm) +/-30%</td>
</tr>
<tr>
<td>Thickness</td>
<td>100 mm (525 +/- 25 μm)</td>
</tr>
<tr>
<td></td>
<td>125 mm (625 +/- 25 μm)</td>
</tr>
<tr>
<td></td>
<td>150 mm (625 +/- 25 μm or 675 +/- 25 μm)</td>
</tr>
<tr>
<td></td>
<td>200 mm (725 +/- 25 μm)</td>
</tr>
<tr>
<td>Primary flat or notch</td>
<td>100 mm (32.5 +/- 2.5 mm)</td>
</tr>
<tr>
<td></td>
<td>125 mm (42.5 +/- 2.5 mm)</td>
</tr>
<tr>
<td></td>
<td>150 mm (47.5 +/- 2.5 mm or 57.5 +/- 2.5 mm)</td>
</tr>
<tr>
<td></td>
<td>200 mm (flat or notch)</td>
</tr>
<tr>
<td></td>
<td>based on SEMI standard</td>
</tr>
</tbody>
</table>
SOI (Silicon On Insulator) Wafers from SEH

SOI wafers are promising semiconductor material for leading edge devices such as low power and high speed LSIs, smart sensors, and smart power devices. Shin-Etsu Handotai (SEH) has been providing wide thickness range of SOI wafers to meet various customers' requirements by using bonding technology.

SOI products from SEH

- UNIBOND® wafers
- Bonded & Polished SOI (BPSOI) wafers

History of SOI wafer development in SEH

SEH started development of SOI wafers in 1988. We began with bonded and polished SOI (BPSOI) wafers by precisely controlled grinding and polishing technology, responding to customers' high quality requirements. For thin SOI wafer (≤ 0.5 μm) production, Smart-Cut® technology was introduced in 1997. UNIBOND® wafers are available now for LSI applications.

Technical Development of SOI Wafers in SEH

- 1988: BPSOI - Thick SOI for BiCMOS, Bipolar and Power devices
- 1994: UNIBOND® - Production technology of thin SOI
Precaution

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